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> PATENT AGENT LARRY N. ANAGNOS

Honorable Commissioner for Patents Washington, D.C. 20231

Attention: Examiner T. Nguyen

Group 2824 Before Final Facsimile No. 703-872-9318

TAKAHASHI et al., U.S. Serial No. 09/974,962

Attorney Docket No. 501.34214R09

FAX RECEIVED

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TECHNOLOGY CENTER 2800

SUBMISSION OF AMENDMENT, SKETCH as attachment, STATEMENT OF STATUS AND SUPPORT FOR CHANGES IN CLAIMS, AND <u>PETITION FOR EXTENSION OF TIME</u>

Sir:

Re:

Applicant hereby submits the attached "Amendment" (10 pgs), "Sketch" (1 pg), "Statement of Status and Support for Changes in Claims" (2 pgs), "Petition for Extension of Time" (1 pg), and "Form PTO-2038" (1 pg) in the above-identified application.

CERTIFICATE OF TRANSMISSION:

I hereby certify that the attached "Amendment" (10 pgs), "Sketch" (1 pg), "Statement of Status and Support for Changes in Claims" (2 pgs), "Petition for Extension of Time" (1 pg), and "Form PTO-2038" (1 pg) are being formally filed in the USPTO via Group 2824 BF Facsimile No. 703-872-9318 on March 26, 2003.

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501.34214R00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

9/14/1-03 ANOON

Applicants:

T. TAKAHASHI et al.

Serial No::

09/974,962

Filed:

October 12, 2001

For:

SEMICONDUCTOR MEMORY

Group:

2824

Examiner:

T. Nguyen

AMENDMENT

Assistant Commissioner for Patents Washington, D.C. 20231

March 26, 2003

Sir:

In response to the Office Action dated November 26, 2002, the period of response for which extension is requested by the attached Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1, 2, 3, 5, 6, 8, 9, 10, 11, 12, 14, 15, 17, 18 and 19 as follows:

1. A semiconductor memory comprising

a plurality of first regions arranged in lattice fashion, each of which corresponds to a memory array including a plurality of main word lines extending in a first direction, a plurality of sets of sub-word lines extending in said first direction, a plurality of pairs of data lines extending in a second direction, perpendicular to said first direction and a plurality of memory cells, each of which is coupled to a corresponding one of said plurality of sub-word lines and a corresponding one of said data lines, one

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